WHAT IS CLAIMED IS:

1. A data processing device comprising:

an electronic processor responsive to a context signal and operable in alternative processing contexts identified by the context signal;

first and second registers connected to said electronic processor to participate in one processing context while retaining information from another processing context until a return thereto; and

a context switching circuit connected to said first and second registers operate to selectively control input and output operations of said registers to and from said electronic processor depending on the processing context.

2. The data processing device of Claim 1 wherein said context switching circuit includes a multiplexer and a control circuit for operating said multiplexer, the processor and one of the registers respectively supplying information for selection by said multiplexer for the other register.

3. The data processing device of Claim 1 wherein the first and second registers both have inputs connected to receive information simultaneously from said processor.

4. The data processing device of Claim 1 wherein said context switching circuit includes an electronic switch and a control circuit wherein said electronic switch is selectively operable by said control circuit to

connect said electronic processor to the first or second register alternatively, depending on the context.

5. The data processing device of Claim 1 wherein said context switching circuit is operable to selectively clock said first and second registers.

6. The data processing device of Claim 5 wherein said first and second registers have outputs connected together and to said processor, and said context switching circuit is further operable to selectively enable an output operation from said first or second register, depending on the context.

7. The data processing device of Claim 1 further comprising a multiplexer, and said first and second registers have respective outputs connected to said multiplexer, said multiplexer operable by said context switching circuit to selectively connect said outputs to said electronic processor.

8. The data processing device of Claim 1 wherein said first register is operated as a main register and said second register is operated as a counterpart register.

9. The data processing device of Claim 1 wherein said first register alternately acts as a main register and then a counterpart register while said second register correspondingly acts as a counterpart register when said first register acts as a main register and then acts as a main register when said first register

acts as a counterpart register.

10. The data processing device of Claim 1 wherein said context signal comprises an interrupt signal and said electronic processor includes an arithmetic logic unit and a data bus coupled to said arithmetic logic unit and to said first and second registers.

11. A data processing device for use with a circuit that produces a digital signal to be processed and an interrupt signal indicating that the digital signal is available for processing, the data processing device comprising:

a data bus;

an arithmetic logic unit connected to said data bus;

an accumulator connected between said arithmetic logic unit and said data bus and a counterpart register for the accumulator; and

switching circuit means for supplying digital values to the accumulator and also holding a currently supplied digital value in the counterpart register upon an occurrence of the interrupt signal while continuing to supply the accumulator with at least a further digital value during an interrupt routine.

12. The data processing device of Claim 11 further comprising a multiplier connected to said data bus; a product register connected between said multiplier and said arithmetic logic unit; a product counterpart register; and additional switching circuit means for supplying digital product values to the product register and holding a currently supplied digital

product value in the product counterpart register when the interrupt signal occurs, while continuing to supply the product counterpart register with at least a further digital product value from the multiplier during the interrupt routine.

13. The data processing device of Claim 11 further comprising additional processing circuitry, a set of first registers interconnecting the data bus, the arithmetic logic unit and the additional processing circuitry, a set of second registers, and switching circuitry connecting the set of second registers respectively to the first registers until the interrupt signal occurs and then temporarily disconnecting the set of second registers from their corresponding first registers when the interrupt signal occurs.

14. A data processing device for use with a circuit that produces a digital signal to be processed and an interrupt signal indicating that the digital signal is available for processing, the data processing device comprising:

a set of first registers and a set of second registers; and

means for executing digital signal processing operations by loading and changing values simultaneously in corresponding ones of the first and second registers so that a value is in a particular one of the first registers and the same value is in a corresponding one of the second registers and for responding to the interrupt signal by executing a set of interrupt operations that load and change at least one value in a

particular one of the first registers leaving the corresponding one of the second registers unchanged.

15. The data processing device of Claim 14 wherein said means for executing includes an arithmetic logic unit and wherein the set of first registers includes an accumulator supplied with a value from the arithmetic logic unit and the set of second registers includes a register corresponding to the accumulator.

16. The data processing device of Claim 14 wherein said means for executing includes a multiplier and the set of first registers includes a product register supplied with a product from the multiplier and the set of second registers includes a register corresponding to the product register.

17. The data processing device of Claim 14 wherein said means for executing includes an address arithmetic unit and the set of first registers includes an index register for supplying an address value to said address arithmetic unit and the set of second registers includes a register corresponding to the index register.

18. A data processing device comprising:

a plurality of registers;

processor means having a program counter and being connected to said plurality of registers for executing a first routine and a second routine involving a program counter discontinuity wherein both routines utilize the plurality of registers; and

a stack associated with said plurality of registers,

the processor means including means operative upon a context change to the second routine for simultaneously pushing the contents of the plurality of registers onto the stack.

19. The data processing device of Claim 18 wherein said processor means further includes means operative upon a return to the first routine for popping said stack to simultaneously load said plurality of registers to allow substantially immediate resumption of the first routine.

20. The data processing device of Claim 19 wherein said second routine is an interrupt service routine.

21. The data processing device of Claim 19 wherein said second routine is a software trap.

22. The data processing device of Claim 19 wherein said second routine is a subroutine.

23. The data processing device of Claim 19 wherein said second routine is a function.

24. The data processing device of Claim 19 further comprising memory means connected to said processor means for storing the second routine.

25. The data processing device of Claim 24 further comprising a hardware interrupt circuit responsive to an interrupt signal and connected to said processor means

wherein said first routine is a main routine and said second routine is an interrupt service routine stored in said memory means, and said means for pushing is responsive to the hardware interrupt circuit to push the contents of the plurality of registers onto the stack upon an occurrence of the interrupt signal.

26. Signal processing apparatus comprising:

circuit means for producing a digital signal to be processed as well as a context signal indicating that the digital signal is available for processing; and

processing means for executing digital signal processing operations and including a set of first registers and a set of second registers connected to participate in one processing context while retaining information from another processing context until a return thereto, and a context switching circuit responsive to said context signal and connected to said sets of first and second registers operative to selectively control input and output operations of said registers to and from said electronic processor depending on the processing context.

27. The signal processing apparatus of Claim 26 wherein said circuit means includes a microprocessor.

28. The signal processing apparatus of Claim 26 wherein said circuit means includes an analog-to-digital converter.

29. The signal processing apparatus of Claim 28

further comprising a digital-to-analog converter connected to convert an output from said processing means to analog form.

30. The signal processing apparatus of Claim 26 wherein said processing means includes a semiconductor chip having a read only memory and a random access memory utilized in said digital signal processing operations.

31. The digital processing apparatus of Claim 30 further comprising an auxiliary memory off-chip and connected to said processing means.

32. Signal processing apparatus comprising:

analog-to-digital converter means for producing a digital signal corresponding to an analog input by a conversion process and for producing an interrupt signal when a conversion is complete;

digital processing means having a memory and a processor connected to said analog-to-digital converter means, said processor responsive to said interrupt signal to enter the digital signal into the memory, the processor including first registers and respectively corresponding second registers to at least some of the first registers, a multiplier and an arithmetic logic unit, said processor including means for simultaneously loading a particular first register and its corresponding one of the second registers with the same digital signal in a first context of operation and then in response to the interrupt signal changing to a second context of operation to selectively load one or more of the first registers leaving the second registers unmodified and

thereby holding the values subsisting from the first context of operation.

33. A method of operating signal processing apparatus used with an analog-to-digital converter that converts an analog input to a digital signal and produces an interrupt signal when a conversion is complete, the method comprising the steps of:

executing digital signal processing operations on a processor according to a first routine and an interrupt routine wherein both routines utilize a plurality of registers; and

associating a stack with said plurality of registers and upon a change to the interrupt routine simultaneously pushing the contents of the plurality of registers onto the stack.

34. The method of Claim 33 further comprising the step of popping said stack to simultaneously load said plurality of registers to allow substantially immediate resumption of the first routine.

35. A motor apparatus comprising:

an electric motor;

means operatively connected to said electric motor for producing a digital signal to be processed as well as a context signal indicating that the digital signal is available for processing; and

digital controller processing means for executing digital signal processing operations and including a set of first registers and a set of second registers connected to participate in one processing context while

retaining information from another processing context until a return thereto, and a context switching circuit responsive to said context signal and connected to said sets of first and second registers operative to selectively control input and output operations of said registers to and from said electronic processor depending on the processing context, said digital controller processing means further including output peripheral means for communicating control signals to said electric motor based on said digital signal processing operations.

36. The motor apparatus of claim 35 wherein said electric motor is a spindle motor for a disk drive.

37. The motor apparatus of claim 35 further comprising an actuator assembly for a disk drive electrically connected to said output peripheral means.

38. The motor apparatus of claim 35 further comprising relays electrically connected to said output peripheral.

39. A speech recognition system comprising:

a microphone;

analog-to-digital converter means for producing a digital signal representative of speech to be processed as well as a context signal indicating that the digital signal is available for processing;

processing means for executing Fourier transform digital signal processing operations and including a set of first registers and a set of second registers connected to participate in one processing

context while retaining information from another processing context until a return thereto, and a context switching circuit responsive to said context signal and connected to said sets of first and second registers operative to selectively control input and output operations of said registers to and from said electronic processor depending on the processing context; and

speech recognition processor means connected to said processing means for executing speech recognition operations in response to the Fourier transform digital signal processing operations.

40. A modem comprising:

analog-to-digital converter means for producing a digital signal representative of a communication channel to be processed as well as a context signal indicating that the digital signal is available for processing; and

processing means for executing digital signal processing operations in digital filtering, demodulation and descrambling, and including a set of first registers and a set of second registers connected to participate in one processing context while retaining information from another processing context until a return thereto, and a context switching circuit responsive to said context signal and connected to said sets of first and second registers operative to selectively control input and output operations of said registers to and from said electronic processor depending on the processing context; and

a universal synchronous asynchronous receiver

transmitter (USART) connected to said processing means for executing communication operations in response to the digital signal processing operations.

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